Claim 21 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Specifically, the phases "wherein the data strobe signal input circuit include" on lines 3-4, were deemed to be unclear. Also, the Examiner indicated that it is not clear how the data signal on line 1 can be "fetched," and how the phrase "data strobe signal input circuit" reads on the preferred embodiment or the drawings.

With regard to the "fetching" of the data signal, claim 21 has been amended to change "fetching" to --for receiving--. With regard to the remaining rejections, Applicant respectfully points out that data strobe signal input circuit includes a differential circuit T_{N1}, T_{N2}, a current mirror 6, a constant current source T_{N3} and a current adjustment transistor T_{N4} as shown in figure 6 and discussed in the specification on page 8, line 21 - page 9, lines 29. The above portions of the specification should clarify the meaning of the phrase "wherein the data strobe signal input circuit include." Also the above portions of the specification should point out how the "data strobe signal input circuit," as recited in the claim reads on the preferred embodiment as disclosed in the specification. Thus, the Applicant submits that claim 21 complies with 35 U.S.C. § 112 and requests withdrawal of the rejection.

Claims 21 was rejected under 35 U.S.C. §102(b) as being anticipated by Kato (U.S. Patent No. 6,100,762). The Applicant respectfully traverses this rejection and submits that Kato fails to disclose, teach or suggest all the features recited in the rejected claims.

Claim 21 of the present invention recites a semiconductor integrated circuit for receiving a data signal in response to rising and falling edges of a data strobe signal including a data strobe signal input circuit which receives the data strobe signal. The data strobe signal input circuit includes a differential circuit having a first transistor and

a second transistor to generate a differential output signal having a logic level, a first gate of the first transistor receiving the data strobe signal, a second gate of the second transistor receiving a reference signal, and sources of the first and second transistor being connected in common and having the same potential. The data strobe signal also includes a current mirror circuit supplying a current to the differential circuit and a constant current source coupled to the sources of the first and second transistors. Finally, the data strobe signal includes a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential output signal of the differential circuit, wherein the current adjustment transistor turns ON and OFF in response to the logic level of the differential output signal such that a falling delay time and a rising delay time of the logic level of the differential output signal are substantially the same.

As a result of the claimed configuration, the circuit applies a differential output signal to the current adjustment transistor without transistors therebetween. Thus, a falling delay time and a rising delay time of the logic level of the differential output signal are substantially the same.

Kato merely discloses that a transistor (M19) is connected in parallel to constant current source (I1) and a gate of the transistor (M14) of output stage (20) (See Kato Fig. 5). The gates of the transistors (M14, M19) receive a differential output signal level-shifted by the transistors (M11, M12). The transistors (M11, M12) merely generate a level-shifted differential output signal applied to transistor (M19). Kato does not teach or suggest that a current adjustment transistor turns ON and OFF in response to the logic level of the differential output signal such that a falling delay time and a rising delay time of the logic level of the differential output signal are substantially the

same, as recited in claim 21 of the present invention. Therefore, claim 21 is patentable over Kato. Thus, the Applicant respectfully requests withdrawal of the rejection and that claim 21 be allowed.

If for any reason the Examiner determines that the application is not in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 1-2300, making reference to Attorney Docket No. 108075-09014.

Respectfully submitted,

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Enclosure: Marked-Up Copy of Claim Amendment

MARKED UP COPY OF THE CLAIM AMENDMENT

21. (Amended) A semiconductor integrated circuit [fetching] for receiving a data signal in response to rising and falling edges of a data strobe signal, comprising:

a data strobe signal input circuit which receives the data strobe signal, wherein the data strobe signal input circuit includes[,]:

a differential circuit having a first transistor and a second transistor to generate a differential output signal having a logic level, a first gate of the first transistor receiving the data strobe signal, a second gate of the second transistor receiving a reference signal, and sources of the first and second transistor being connected in common and having the same potential,

a current mirror circuit supplying a current to the differential circuit,

a constant current source coupled to the sources of the first and second transistors, and

a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential output signal of the differential circuit, wherein the current adjustment transistor turns ON and OFF in response to the logic level of the differential output signal such that a falling delay time and a rising delay time of the logic level of the differential output signal are substantially the same.